Analog MMICs for Millimeter-Wave Applications Based on a Commercial 0.14-μm pHEMT Technology

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***Abstract*—This paper describe recent results obtained from the monolithic—microwave integrated-circuit design activity at Chalmers University, Göteborg, Sweden. The goal is to design all circuits needed for the front end of a 60-GHz wireless local area network and to build various system demonstrators. Some recent experimental results from this activity like different 60-GHz amplifiers, a general-purpose IF amplifier, a 60-GHz resistive mixer, and frequency multipliers are reported in this paper. Parameters such as the gain, conversion loss, noise figure, dc-power dissipation, as well as the model used in the simulations are reported and discussed.**

***Index Terms*—Amplifter, frequency mixer, frequency multiplier, MMIC, millimeter waves.**

I. Introduction

THE millimeter-wave bands have in recent years gained increased interest for wireless applications due to its wide-frequency spectrum, high data rate, compact-sized hardware solutions, and the possibility of interference-free system configurations. The use of 60 GHz for such applications is very interesting due to the oxygen absorption in the atmosphere, and the presence of "open" nonrestricted frequency bands. Application areas include mobile wide-band cellular systems, fixed wireless broad-band access systems, wireless local area networks, and wireless vehicle and traffic information systems. Many research institutes and universities have an activity in this area such as the University of Surrey, Surrey, U.K., Helsinki University, Helsinki, Finland, Nokia, Helsinki, Finland, Ferdinand Braun Institute, Berlin, Germany, Alcatel-SEL, Stuttgart, Germany, France Telecom, France, Thomson-CSF Detexis, France, OPTO+, France, NMRC, Cork, Ireland, Farran Technologies Ltd. Cork, Ireland, NEC Corporation, Japan, NTT DoCoMo, Yokosuka, Japan, Central Research Laboratory (CRL), Yokosuka Japan, Fujitsu Laboratories Ltd., Atsugi, Kanagawa, Japan, Kansai Electronics Research Laboratories, NEC Corporation, Otsu, Shiga, Japan, Tohoku University, Sendai, Japan. Chalmers University of Technology, Göteborg, Sweden, The Royal Institute of Technology, Stockholm, Sweden, The Swedish Defence Research Agency (FOI), Linköping, Sweden, and Ericsson Microwave Systems AB, Mölndal, Sweden, have started a multidisciplinary activity to cover problem areas such as circuit design, system design and simulation, antennas, applications, and packaging and interconnects. One activity is to investigate a GaAs-based monolithic-microwave integrated-circuit (MMIC) technology and to find suitable circuit solutions for various system demonstrators. Circuits such as various amplifiers, frequency mixers, frequency multipliers, frequency dividers, modulators, oscillators, and switches are also studied.

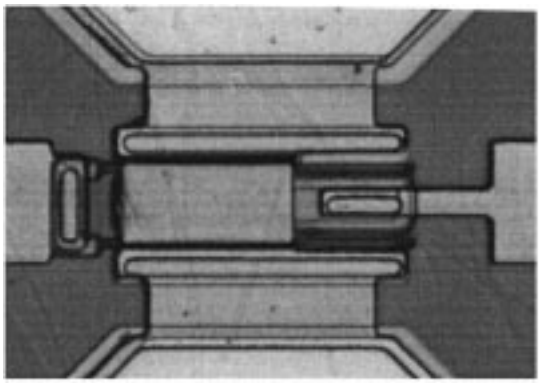

Fig. 1. Layout of a 2 × 50 μm gatewidth device.

II. MMIC Technology

In this study, we use a commercial foundry process from OMMIC,[1] France, based on a double delta doped layer structure for high-performance pseudomorphic high electron-mobility transistor (pHEMT) devices utilizing high drain current density with high breakdown voltage. The photo of a 100-μm gatewidth high electron-mobility transistor (HEMT) device is shown in Fig. 1. The gates are mushroom shaped for low gate resistance with a gate length of 0.14 μm. DC characteristics were measured with an HP 4156 parameter analyzer. The $I_{\rm ds}$–$V_{\rm ds}$ and $I_{\rm ds}$–$V_{\rm gs}$ characteristics is plotted in Figs. 2 and 3. The measurements show a maximum current density of approximately 700 mA/mm and a maximum transconductance of 700 mS/mm. The $f_{\rm t}$ and $f_{\rm max}$ were characterized on the same test device, i.e., 100 and 180 GHz, respectively, was obtained. Circuits like

Manuscript received March 5, 2001. This work was supported by the Chalmers Center for High Speed Technology (CHACH), by The Swedish Agency for Innovation Systems (VINNOVA), by the Foundation for Strategic Research (SSF), by the Swedish Defence Material Administration (FMV), and by the European Space Agency.

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Publisher Item Identifier S 0018-9480(01)09396-6.

[1]Process D01PH from OMMIC, Limeil-Brevannes, France.

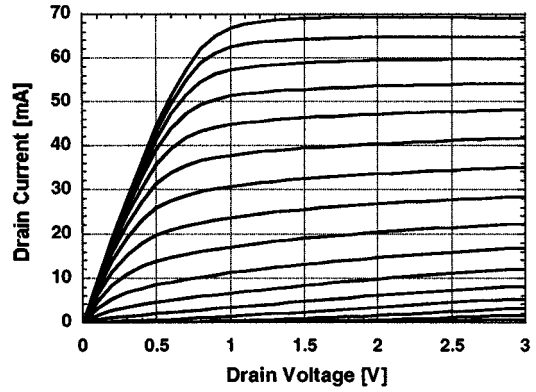

Fig. 2. Measured $I_{\rm ds}$–$V_{\rm ds}$ characteristic as $V_{\rm gs}$ is varied from -1 to $+0.5$ V with 0.1-V steps.

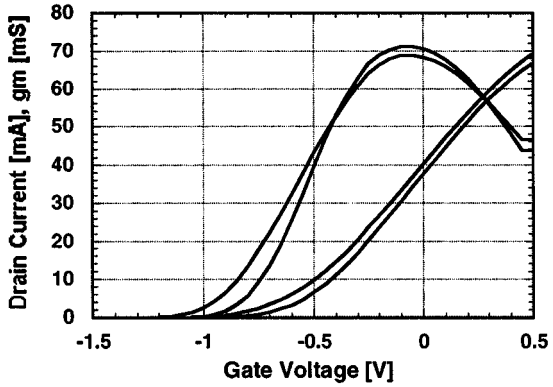

Fig. 3. Measured $I_{\rm ds}$–$V_{\rm gs}$ characteristic at $V_{\rm ds}$ equal to 1 and 2 V.

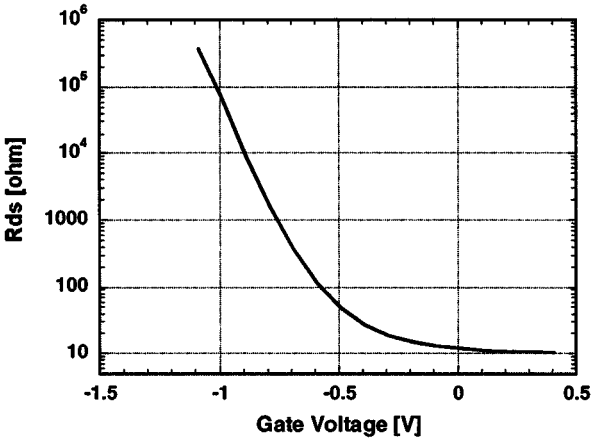

Fig. 4. Measured $R_{\rm ds}$–$V_{\rm gs}$ characteristic at $V_{\rm ds} = 0.05$ V.

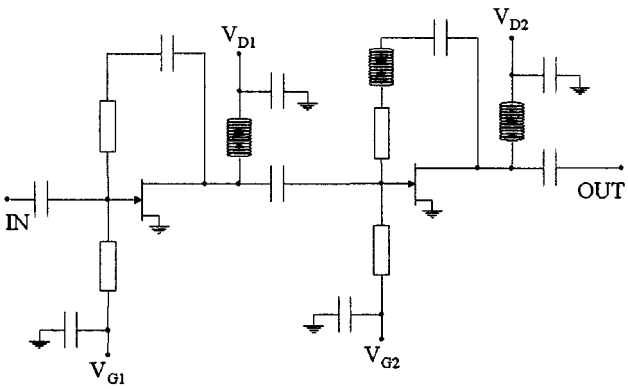

Fig. 5. Circuit diagram of the feedback amplifier.

switches, resistive mixers, and attenuators utilize the unsaturated part of the $I_{\rm ds}$–$V_{\rm ds}$ characteristic, at low drain–source voltage, where the device works as a gate–voltage-controlled resistor. In this regime, the $R_{\rm ds}$–$V_{\rm gs}$ dependence is important [17]; it is shown in Fig. 4 for the 100-μm test device. The minimum $R_{\rm ds}$ is 1.0 $\Omega \cdot$ mm. S-parameters and noise parameters were also measured based on an HP 8510C and an ATN NP5 on-wafer noise parameter test system on a variety of HEMTs with varying sizes as a function of bias. From these measurements, we have extracted large-signal models and bias-dependent noise models to complement the foundry models. Our models are described in [1] and [2].

III. IF/Broad-Band Amplifiers

Different amplifiers based on grounded gate and resistive feedback topologies were studied. The *parallel resistive feedback amplifier* was found to be particularly interesting since it can give an attractive combination of key parameters such as gain, gain flatness, input and output standing-wave ratio (SWR), noise figure, linearity, output power density, dc-power dissipation, and circuit area. The theoretical foundation of this circuit is described very well in the literature [3]–[7]. The feedback is utilized by connecting a resistor between the gate and drain. If the transistor is represented by a simple model consisting of only a voltage-controlled current generator with the transconductance g_m, simple circuit analysis gives the relation between the transistors transconductance g_m, the feedback resistance $R_{\rm f}$, and the characteristic impedance Z_0, assuming $S11 = S22 = 0$ as follows:

$$R_{\rm f} = g_m \cdot Z_0^2.$$

The gain S_{21} of such an amplifier is then

$$S_{21} = \frac{Z_0 - R_{\rm f}}{Z_0} = 1 - g_m \cdot Z_0.$$

The above expression is, of course, a simplification, which nevertheless gives a basic understanding and an estimation of the gain that can be achieved by a single-stage feedback amplifier. In the simulation, we use a full equivalent-circuit model, which also include the appropriate noise sources. The amplifier was designed with the goals to give a minimum gain of 20 dB in a frequency range of 2–20 GHz, with a noise figure less than 3 dB. In order to achieve this, two transistor stages were cascaded. The gates and drains are accessible by dc probes. This enables an experimental investigation of the bias tradeoff in terms of gain, output power, noise figure, etc. The circuit diagram of the feedback amplifier is shown in the Fig. 5. Both transistors have a gatewidth of 4 $\times$ 50 μm yielding a maximum transconductance of nominally 140 mS. The feedback network is a resistance of 250 Ω in series with a 1-pF capacitor. The second stage has an inductor in the feedback path in order to give the amplifier a gain boost at the high end of the frequency range. Both drains are connected to the supply voltage through a 4-nH

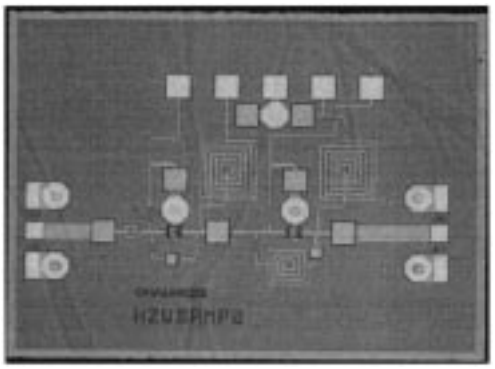

Fig. 6. Feedback amplifier.

inductor. The gates are biased through 500-Ω gate resistors. The input and output are dc isolated through coupling capacitances. Input and output coplanar-waveguide (CPW) probes and pads for bias are provided to facilitate "on wafer" characterization of the amplifier. The total chip area is 2×1.5 mm^2, while the active area of the amplifier is approximately 1 mm^2. The layout of the MMIC in shown in Fig. 6. The small-signal parameters of the devices were obtained by means of the cold-FET method with an equivalent circuit that has been described elsewhere [8]. In addition, the noise parameters of both transistors were measured at different bias conditions. From the noise measurements, the Pospieszalski parameters, drain temperature $T_{\rm D}$, and gate temperature $T_{\rm G}$ [9] were initially extracted and then tuned by direct optimization with the gradient method. Once the optimized values were calculated, a nonlinear curve fitting was made to obtain an analytical expression for both $T_{\rm G}$ and $T_{\rm D}$ as a function of the drain current density. The most accurate prediction of the noise parameters was achieved by assuming a linear dependence for $T_{\rm G}$ and a hyperbolic dependence with a current density offset for $T_{\rm D}$ as follows:

$$T_{\rm D} = T_{\rm D0} \cosh \frac{J_{\rm D} - J_0}{J_1}$$

where $T_{\rm D0}$, J_0 and J_1 are fitting factors. The accuracy of this expression has also been verified at bias points near pinchoff operation. Figs. 7 and 8 show the calculated drain and gate temperatures for drain voltages of 1 and 2 V, and different drain current densities. Two transistors of different gatewidths were measured to verify the scalability of the model. As can be observed in Fig. 4, the discrepancies between the drain temperatures of both devices remain low enough to safely apply the above expression with the same fitting factors to both devices.

The MMIC was characterized by using a vector network analyzer, i.e., HP 8510C, and an "on-wafer" noise parameter measurement system (ATN). The simulated and measured amplifier gain and minimum noise figure ($F_{\rm min}$) are given in Fig. 9 for the optimum bias conditions. The bandwidth is approximately 20 GHz and the minimum noise figure was about 2.6 dB. Simulation were performed by using a commercially available computer-aided design (CAD) tool.[2] The output power versus input power and drain supply voltage was also investigated by using harmonic balance simulations and experimental verification at different frequencies. In Fig. 10, the simulated and measured output power versus input power characteristic is shown at a drain supply voltage $V_{\rm dd}$ of 1.5, 2, 3, and 4 V at 10 GHz. The maximum measured output power is approximately 19 dBm at an input power of 0 dBm and 2.5-dB compression. From Fig. 10,

[2]MDS, Microwave Design System, Agilent Technologies, Palo Alto, CA.

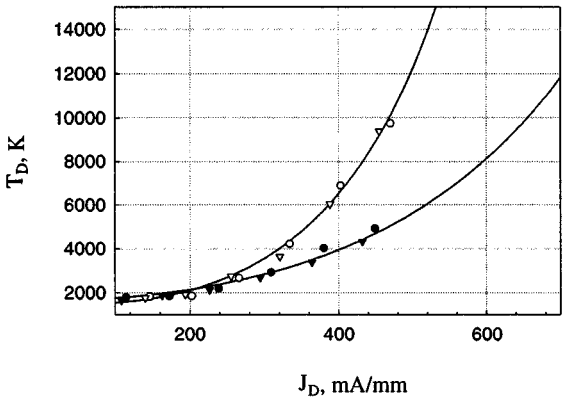

Fig. 7. Optimized and fitted (lines) values of the Pospieszalski drain temperature. Circles: transistor with 100-μm and triangles with 200-μm gatewidth. Open symbols correspond to $V_{\rm D} = 2$ V, solid symbols to $V_{\rm D} = 1$ V.

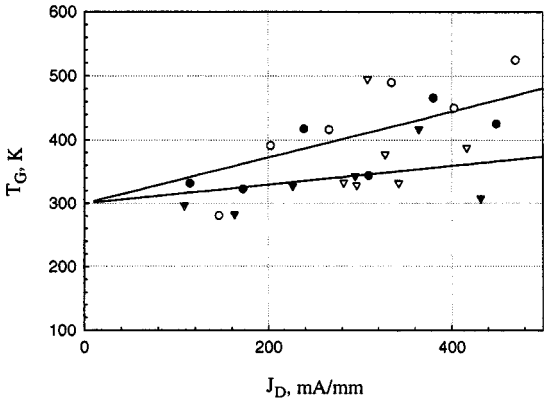

Fig. 8. Optimized and fitted (lines) values of the Pospieszalski gate temperature. Circles: transistor with 100-μm and triangles with 200-μm gatewidths. Open symbols correspond to $V_{\rm D} = 2$ V, solid symbols to $V_{\rm D} = 1$ V.

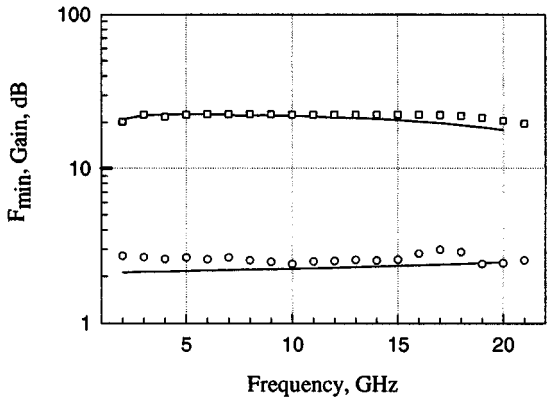

Fig. 9. Measured (open symbols) and simulated (lines) minimum noise figure and gain of the wide-band amplifier versus frequency. Drain bias of the first transistor $V_{\rm D1} = 1.5$ V, for the second transistor $V_{\rm D2} = 1.5$ V, gate biases $V_{\rm G1} = 0$ V, $V_{\rm G2} = 0$ V.

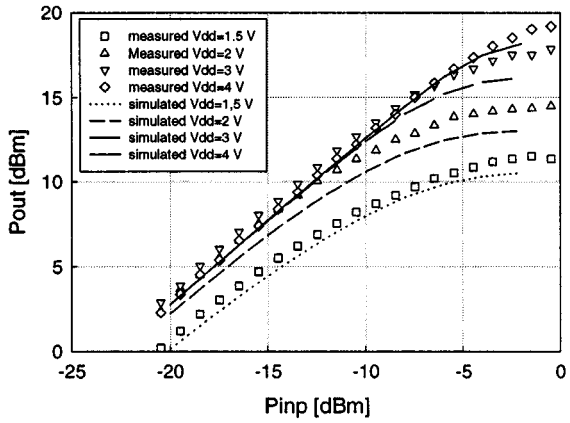

Fig. 10. Output power versus input power characteristics at different values of drain bias at 10 GHz.

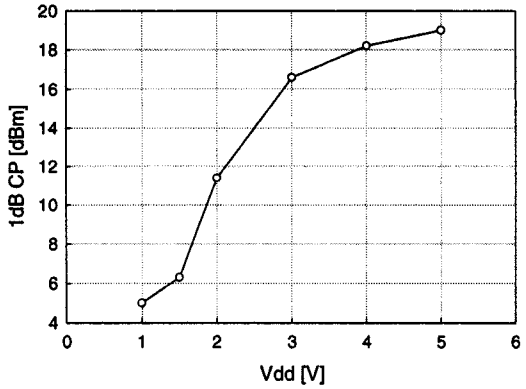

Fig. 11. Measured 1-dB compressed power versus drain bias at 10 GHz.

we can also obtain the 1-dB compression point versus $V_{\rm dd}$. This relation is plotted in the Fig. 11. As can be noticed from this figure, the 1-dB compression power increases quite rapidly at $V_{\rm dd}$ up to 3 V. Above 3 V, the increase in the 1-dB compressed power is much smaller. The efficiency $\eta = P_{\rm out}/P_{\rm DC}$ is 20% at $V_{\rm dd} = 3$–4 V.

IV. 60-GHz Amplifiers

Different designs of amplifiers were evaluated with different transistor gatewidths. Two designs are shown below (see Figs. 12 and 13). Design 1 is a three-stage amplifier utilizing 2×15 μm gatewidth devices for minimum dc-power dissipation and low-noise applications. The other design is also three-stage, but based on 4×15 μm gatewidth devices for higher output power.

The first design (HZAMP60) is designed to have the minimum noise at 60 GHz, which is accomplished by using an input stub for Γ-opt matching. A matching stub is also used at the output in order to match the output port at 60 GHz. The gates and drains can be biased individually in order to investigate the bias dependence. Resistors are placed in the bias lines to the gates and drains to achieve electrical stability. The amplifiers were measured by using an HP8510XF network analyzers covering 2–85 GHz in one frequency sweep; all measurements were performed by using coplanar probes. Both amplifiers were found to

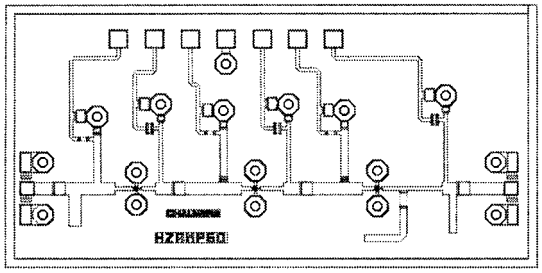

Fig. 12. Layout of 60-GHz amplifiers (design 1, HZAMP60).

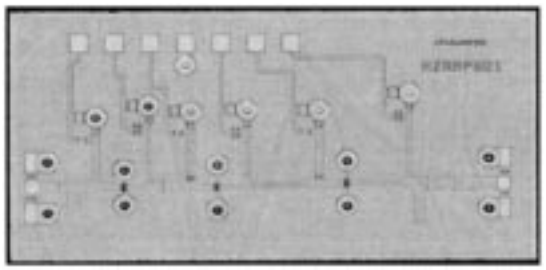

Fig. 13. Layout of 60-GHz amplifiers (design 2, HZAMP601).

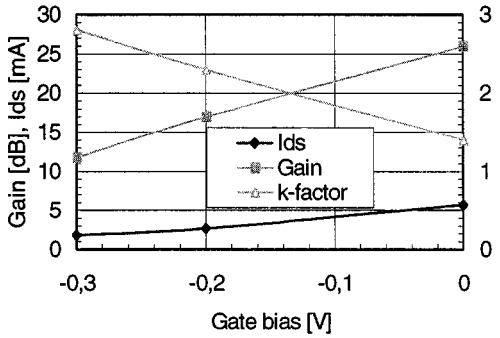

Fig. 14. Gain, drain current per stage, and k-factor (right axis) versus gate bias for HZAMP60.

be stable (no signs of oscillations could be noticed) for all possible bias conditions. At a bias of $V_{\rm dd} = 3$ V and a drain current of 2.7 mA per stage, the measured mid-band gain is 17 dB. The gain is increasing with increasing current (at 4 mA) and the gain is increased to 21.6 dB. The amplifier is also unconditionally stable at $V_{\rm dd} = 3$ V for all bias points, i.e., the amplifier cannot oscillate for *any* possible passive termination at the input and output. A typical bias point could be $V_{\rm dd} = 3$ V and a drain current of approximately 3 mA per stage yielding a total dc-power dissipation of 27 mW; the gain is then 17 dB and the 3-dB bandwidth is $57–60.8 = 3.8$ GHz. The k-factor is 2.3 for this case. The observed gain, drain current, and stability factor is shown in Fig. 14 as a function of gate bias.

The second design (HZAMP601) uses 4×15 μm gatewidth devices, which increases the maximum output power compared to the previous design, $P_{\rm out} = 12$ dBm was measured at $V_{\rm dd} = 2$ V. At $V_{\rm dd} = 3$ V and $I_{\rm dd} = 9$ mA/stage, the gain is 17.6 dB and the 3-dB bandwidth is 54.3–60 GHz, i.e., 5.7 GHz. If the current is increased to 12 mA, the maximum gain increase to 20.4 dB with a 3-dB bandwidth of 54.0–59.75 GHz; the k-factor is then 2.2. The noise figure is not measured yet.

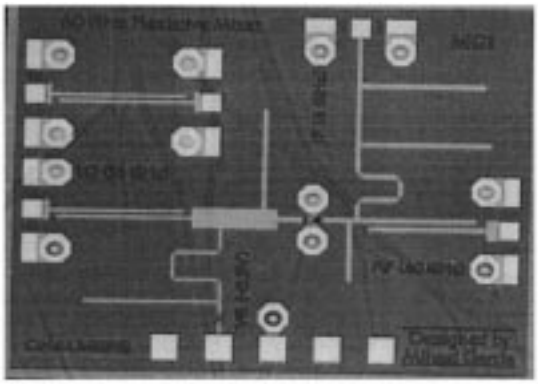

Fig. 15. 60-GHz single-ended HEMT resistive mixer.

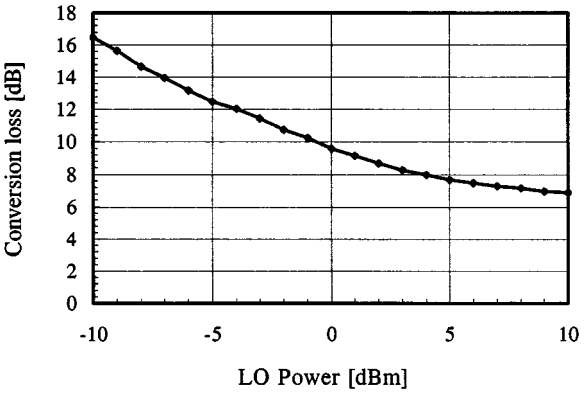

Fig. 16. Measured optimum conversion loss versus LO power at 60 GHz.

V. Frequency Converters

Several different millimeter-wave frequency up/down converters, based on resistive mixing in the channel of the HEMT, working at a center frequency of 60 GHz were designed, both single ended and balanced. The resistive mixer was first described by Maas as an X-band mixer [10]. Several different mixers have also been realized mainly based on InP HEMTs by our group [11]–[14]. By utilizing InP HEMTs, lower conversion loss at much less local oscillator (LO) power is typically achieved compared to GaAs-based resistive mixers [15]. Nevertheless, the technology used in this study is well suited for resistive mixing due to the low specific on resistance of the active devices. The layout of a single-ended mixer is shown in Fig. 15. The LO signal is connected to the left CPW pad, the RF to the right CPW pad, and the IF to the upper pad. The LO signal is applied to the gate, modulating the drain–source resistance of the HEMT. If an RF signal is applied to the drain, then the drain current will have a spectral component corresponding to the difference frequency $f_{\mathrm{LO}} - f_{\mathrm{RF}}$. This signal is extracted through the IF filter. The IF filter is realized with open stubs. The conversion loss, i.e., the ratio between the RF and IF power, can be minimized by adjusting the shape of the resistance waveform. This is done at a particular LO power by optimizing the gate bias voltage. It is possible to bias the gate through the second bias pad at the bottom of the figure. According to the simulations, a conversion loss of 7.7 dB is obtained at an LO power of 5 dBm. The 60-GHz measured optimum conversion loss as a function of the LO power is shown in Fig. 16. The conversion loss is optimum at a gate voltage of -0.5 V in good agreement with simulations. The conversion loss is 8 dB, at an LO power of only 3 dBm. This is normally sufficient for down-converter applications in combination with a low-noise high-gain amplifier. This mixer is also quite broad band, and the conversion-loss variation is less than 1 dB for an RF signal between 50–62 GHz.

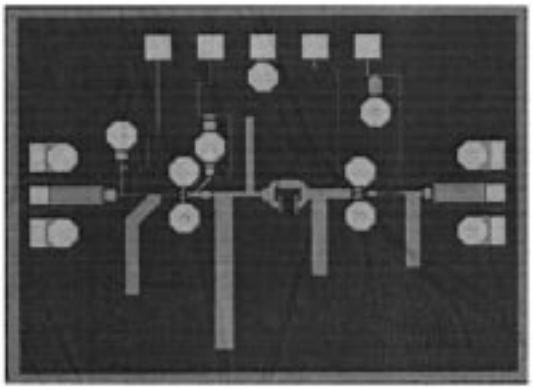

Fig. 17. 30–60-GHz doubler chip.

VI. Frequency Multipliers

Frequency multipliers might be an alternative for the LO generation in the millimeter-wave bands. Instead of using a fundamental frequency oscillator, the oscillator can be designed at a lower frequency and then multiplied. Several different frequency multiplier designs were evaluated like 30–60-GHz doublers, 8–32-GHz quadruplers, 16–32-GHz doublers, etc.

Different 30–60-GHz multipliers have been designed; thus far, one has been characterized. The chip presented here is shown in Fig. 17. This frequency multiplier is based on two transistors; the first is used for harmonic generation, the second as an amplifier. Suppression of the fundamental frequency component is achieved by "shorting" the drain through a short transmission line, a MMIC frequency-doubler topology that was first described in [18]. This type of frequency doubler has the advantages of a small circuit area, low power consumption, and good suppression of unwanted harmonics. The measured output power is 6 dBm at an input power of 5 dBm. The 3-dB bandwidth is 48–60 GHz. The fundamental frequency suppression is 20–30 dB within the band and the dc-power consumption is 275 mW; we believe, however, that this power consumption can be reduced considerably by redesign. The frequency response is shown in Fig. 18.

An 8–32-GHz frequency quadrupler was also designed, fabricated, and characterized based on the same circuit topology as the previous one. It consists of two cascaded frequency doublers, each transistor has a gatewidth of 60 μm. The chip layout and the measured output versus input power characteristics at 8 GHz are shown in Figs. 19 and 20. The maximum output power is 1.2 dBm. This quadrupler has a maximum conversion gain of 1 dB. The 3-dB bandwidth at 0-dBm input power is 29.5–33.2 GHz. The dc-power consumption P_{dc} depends on the excitation level since the devices are biased close to pinchoff. At the maximum output power, the dc-power consumption is approximately 100 mW. Measurements shows that the output power is compressed at input powers above -1 dBm.

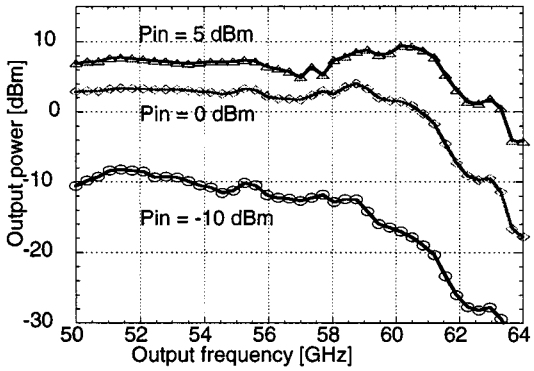

Fig. 18. Frequency response of the doubler.

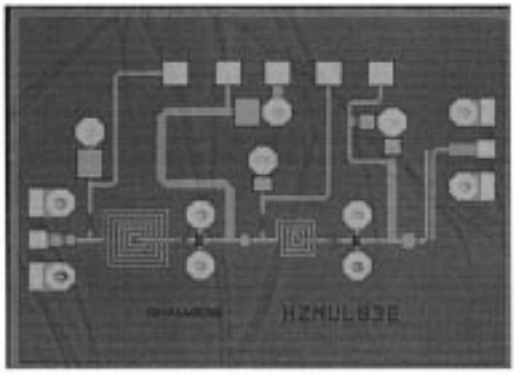

Fig. 19. 8–32-GHz quadrupler chip.

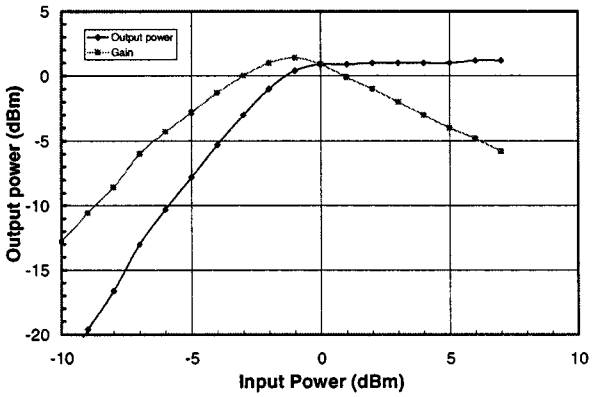

Fig. 20. $P_{\rm out}$ versus $P_{\rm in}$ characteristics and conversion gain versus input power at 8 GHz.

VII. Discussion and Conclusion

MMICs for 60-GHz wireless applications like amplifiers, frequency multipliers, and frequency mixers have been designed, fabricated, and characterized. The resistive feedback amplifier was found to have very attractive data with the chosen MMIC technology, which makes it very suitable as a broad-band, general-purpose, medium-power, and low-noise amplifier. For *battery-operated systems*, the dc-power consumption is a critical parameter. The power required to pump the frequency converters is also then a critical parameter since it usually requires power amplification. The efficiency of such amplifiers is normally of the order of 20%, thus, a low LO power requirement would be an attractive parameter. The 60-GHz amplifiers reported here with 30-μm gatewidth transistors perform well (17-dB gain, three stage) at a power dissipation of 27 mA. It was shown that by doubling the gatewidth, the bandwidth was increased by approximately 50%, but the power dissipation was more than doubled for the same gain. Since it is zero, the resistive mixer is an excellent choice if the dc-power dissipation is an important parameter. Efficient conversion can be achieved with a low LO power; 0–5 dBm is sufficient for most applications. The frequency multipliers require most dc power, approximately 50 mW for a frequency doubling. One possible approach would be to minimize the gatewidth of the transistors and to use a post-amplifier, utilizing transistors with a minimum gatewidth. Another approach to investigate further is the resistive FET/HEMT doubler [19], [20]. This circuit is similar to a resistive FET mixer, but the same signal is applied both at the gate and drain with a phase difference that maximizes the conversion efficiency. The multiplied input signal is extracted from the drain through a bandpass filter. A conversion loss of 4–5 dB can be expected.

Acknowledgment

The authors wish to acknowledge I. Angelov, Chalmers University of Technology, Göteborg, Sweden, J. Stenarson, Chalmers University of Technology, Göteborg, Sweden, K. Yhland, Chalmers University of Technology, Göteborg, Sweden, M. Hasselblad, Ericsson Microwave Systems, Mölndal, Sweden, and J. Miranda, University Complutense of Madrid, Madrid, Spain, for their contributions to the MMIC project. The authors are highly appreciative and acknowledge the support of E. Kollberg, Chalmers University of Technology, Göteborg, Sweden, T. Lewin, Ericsson Microwave Systems, Mölndal, Sweden, J. Noreus, Ericsson Microwave Systems, Mölndal, Sweden, A. Filipsson, Ericsson Microwave Systems, Mölndal, Sweden, C. Stoij, Moheda, Sweden, K. Jarl, Combitech Systems AB, Mölndal, Sweden, G. Ericsson, Swedish Defence Material Administration, Stockholm, Sweden, T. Larsson, Swedish Defence Material Administration, Stockholm, Sweden, T. Närhi, European Space and Technology Centre, Noodwijk, The Netherlands, D. Antsos, Jet Propulsion Laboratory, Pasadena, CA, D. Rutledge, California Institute of Technology, Pasadena, G. Lövestam, Chalmers University of Technology, Göteborg, Sweden, and the people at OMMIC, Limeil-Brevannes, France. The authors further acknowledge Agilent Technologies, Palo Alto, CA, for their software donation.

References

[1] J. M. Miranda, H. Zirath, P. Sakalas, M. García, and J. L. Sebastián, "Microwave noise modeling of HEMT devices under low power consumption operation," in *IEEE MTT-S Int. Microwave Symp. Dig.*, vol. 2, Boston, MA, 2000, pp. 1233–1236.

[2] I. Angelov, H. Zirath, and N. Rorsman, "A new empirical nonlinear model for HEMT and MESFET devices," *IEEE Trans. Microwave Theory Tech.*, vol. 40, pp. 2258–2266, Dec. 1992.

[3] G. Gonzales, *Microwave Transistor Amplifiers*. Englewood Cliffs, NJ: Prentice-Hall, 1997, pp. 333–342.

[4] R. S. Pengelly, *Microwave Field-Effect Transistors—Theory, Design and Applications*, 2nd ed. New York: Wiley, 1986, pp. 210–216.

[5] P. H. Ladbroke, *MMIC Design: GaAs FET's and HEMT's*. Norwood, MA: Artech House, 1989, pp. 279–287.

[6] F. Perez and V. A. Ortega, "A graphical method for the design of feedback networks for microwave transistor amplifiers: Theory and applications," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-30, pp. 976–981, July 1982.
[7] K. B. Niclas, "The matched feedback amplifier: Ultrawideband microwave amplification with GaAs MESFET's," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-28, pp. 285–294, Apr. 1980.
[8] N. Rorsman, M. Garcia, C. Karlsson, and H. Zirath, "Accurate small-signal modeling of HFET's for millimeter-wave applications," *IEEE Trans. Microwave Theory Tech.*, vol. 44, pp. 432–437, Mar. 1996.
[9] M. W. Pospieszalski, "Modeling of noise parameters of MESFET's and MODFET's and their frequency and temperature dependence," *IEEE Trans. Microwave Theory Tech.*, vol. 37, pp. 1340–1350, Sept. 1989.
[10] S. A. Maas, "A GaAs MESFET mixer with very low intermodulation," *IEEE Trans. Microwave Theory Tech.*, vol. 35, pp. 425–429, Apr. 1987.
[11] I. Angelov, H. Zirath, N. Rorsman, C. Karlsson, and R. Weikle, "A resistive mixer for the F-band," in *Proc. IEEE MTT-S Int. Microwave Symp. Dig.*, 1993, pp. 787–790.
[12] H. Zirath, I. Angelov, and C. Karlsson, "An LO-rejecting balanced up converter for communication systems," in *Proc. European Microwave Conf.*, Prague, Czech Republic, 1996, pp. 104–107.
[13] K. Yhland, N. Rorsman, and H. Zirath, "A novel single device balanced resistive HEMT mixer," *IEEE Trans. Microwave Theory Tech.*, vol. 43, pp. 2863–2867, Dec. 1995.
[14] C. Karlsson, N. Rorsman, and H. Zirath, "A monolithically integrated F-band resistive InAlAs/InGaAs/InP HFET mixer," *IEEE Microwave Guided Wave Lett.*, vol. 5, no. 11, pp. 394–395, 1995.
[15] H. Zirath, M. Sironen, N. Rorsman, C. Karlsson, and I. Angelov, "A millimeter-wave AlInAs–GaInAs HFET-based harmonic mixer," in *Proc. European Microwave Conf.*, Bologna, Italy, Sept. 1995, pp. 294–298.
[16] H. Zirath, N. Rorsman, C. Y. Chi, and G. Rebeiz, "A 40-GHz integrated quasi-optical slot HFET mixer," *IEEE Trans. Microwave Theory Tech.*, vol. 42, pp. 2492–2497, Dec. 1994.
[17] H. Zirath, "Millimeter-wave mixers with focus on resistive FET-mixers," presented at the IEEE MTT-S New Mixer Technol. Workshop, San Francisco, CA, 1996.
[18] H. Zirath, L. Landen, and C. Fager, "An active millimeter wave MMIC frequency doubler with high spectral purity and low power consumption," in *GaAs European Microwave Conf.*, Munich, Germany, 1999, pp. 33–36.
[19] M. Jonsson, H. Zirath, and K. Yhland, "A new FET frequency multiplier," in *IEEE MTT-S Int. Microwave Symp. Dig.*, vol. 3, June 1998, pp. 1427–1430.
[20] M. Jonsson, "Resistive FET Frequency Multipliers for Micro- and Millimeter Waves," Licentiate Eng. thesis, Dept. Microelectron., Chalmers Univ. Technol., Göteborg, Sweden, 1999.

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Christian Fager, photograph and biography not available at time of publication.

Mikael Garcia, photograph and biography not available at time of publication.

Paulius Sakalas, photograph and biography not available at time of publication.

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